CLAIMS:

1-31. (Canceled)

32. (Previously Presented) A method comprising:

terminating a plurality of applications running in an operating system environment that supports dynamic removal of a first processor cluster from a plurality of processor clusters, the first processor cluster including a first plurality of processors and a first interconnection controller interconnected using a point-to-point architecture;

identifying the first processor cluster for removal;

flushing a plurality of caches associated with the first processor cluster;

modifying a plurality of routing tables associated with each processor cluster to reflect removal of the first processor cluster;

disabling link layer communications associated with the first processor cluster, wherein the first processor cluster is disconnected after disabling link layer communications associated with the first processor cluster;

maintaining physical layer communications associated with the first processor cluster to allow connection of a replacement processor cluster.

33. (Previously Presented) The method of claim 32, wherein a fence bit is written by a service processor.

34. (Previously Presented) The method of claim 32, wherein a fence bit is written by a JTAG interface associated with a processor.

35. (Previously Presented) The method of claim 32, wherein the first cluster of processors and a second cluster of processors share a single virtual address space.

36. (Previously Presented) The method of claim 35, wherein the second cluster of processors includes a second interconnection controller.

37. (Previously Presented) The method of claim 36, wherein the second interconnection controller includes a physical layer enable indicator.

38. (Previously Presented) The method of claim 36, wherein the second interconnection controller includes a fence indicator configurable to prevent the transmission of logical packets between the first interconnection controller and the second interconnection controller.

39. (Previously Presented) The method of claim 36, wherein the second interconnection controller includes a reinitialization indicator configurable to direct the second interconnection controller to reinitialize the link.

40-47. (Canceled)

48. (Previously Presented) An apparatus comprising:

means for terminating a plurality of applications running in an operating system environment that supports dynamic removal of a first processor cluster from a plurality of processor clusters, the first processor cluster including a first plurality of processors and a first interconnection controller interconnected using a point-to-point architecture;

means for identifying a first processor cluster for removal;

means for flushing a plurality of caches associated with the first processor cluster;

means for modifying a plurality of routing tables associated with each processor cluster to reflect removal of the first processor cluster;

means for disabling link layer communications associated with the first processor cluster, wherein the first processor cluster is disconnected after disabling link layer communications associated with the first processor cluster;

means for maintaining physical layer communications associated with the first processor cluster to allow connection of a replacement processor cluster.

49. (Previously Presented) The apparatus of claim 48, wherein a fence bit is written by a service processor.

50. (Previously Presented) The apparatus of claim 48, wherein a fence bit is written by a JTAG interface associated with a processor.

51. (Previously Presented) The apparatus of claim 48, wherein the first cluster of processors and the second cluster of processors share a single virtual address space.